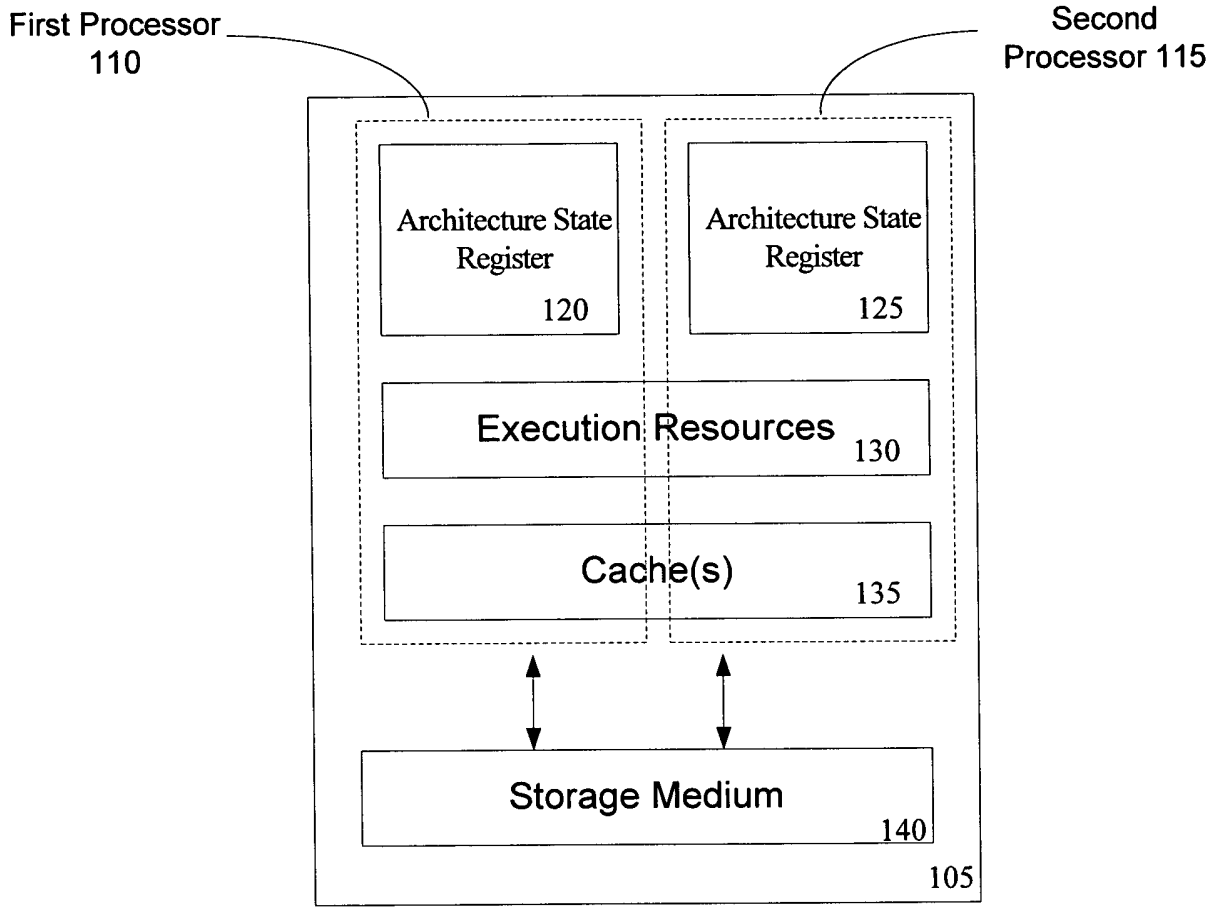
First Processor 110
Second Processor 115
Architecture State Register 120
Architecture State Register 125
Execution Resources 130
Cache(s) 135
Storage Medium 140
105

FIG. 1

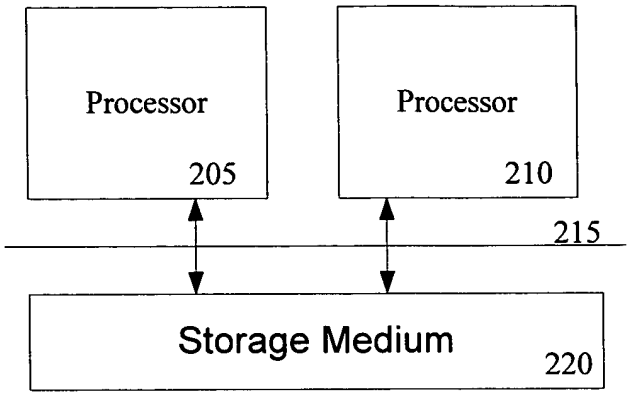
Processor
205
Processor
210
215
Storage Medium
220

FIG. 2a

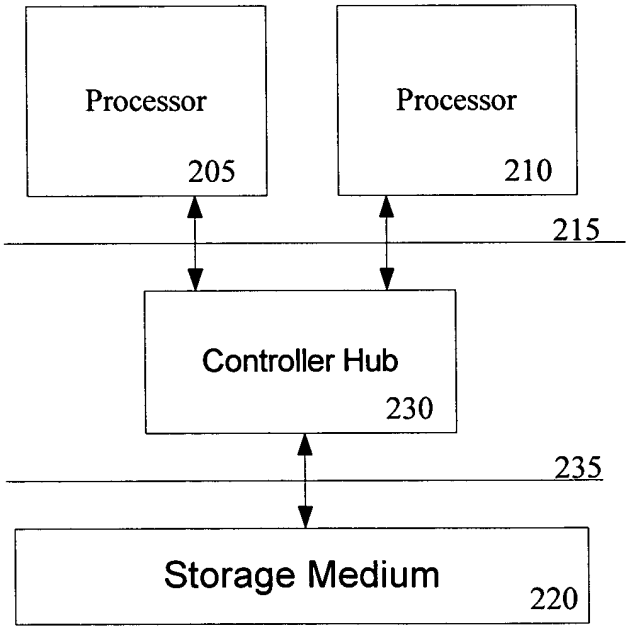
Processor
205
Processor
210
215
Controller Hub
230
235
Storage Medium
220

FIG. 2b

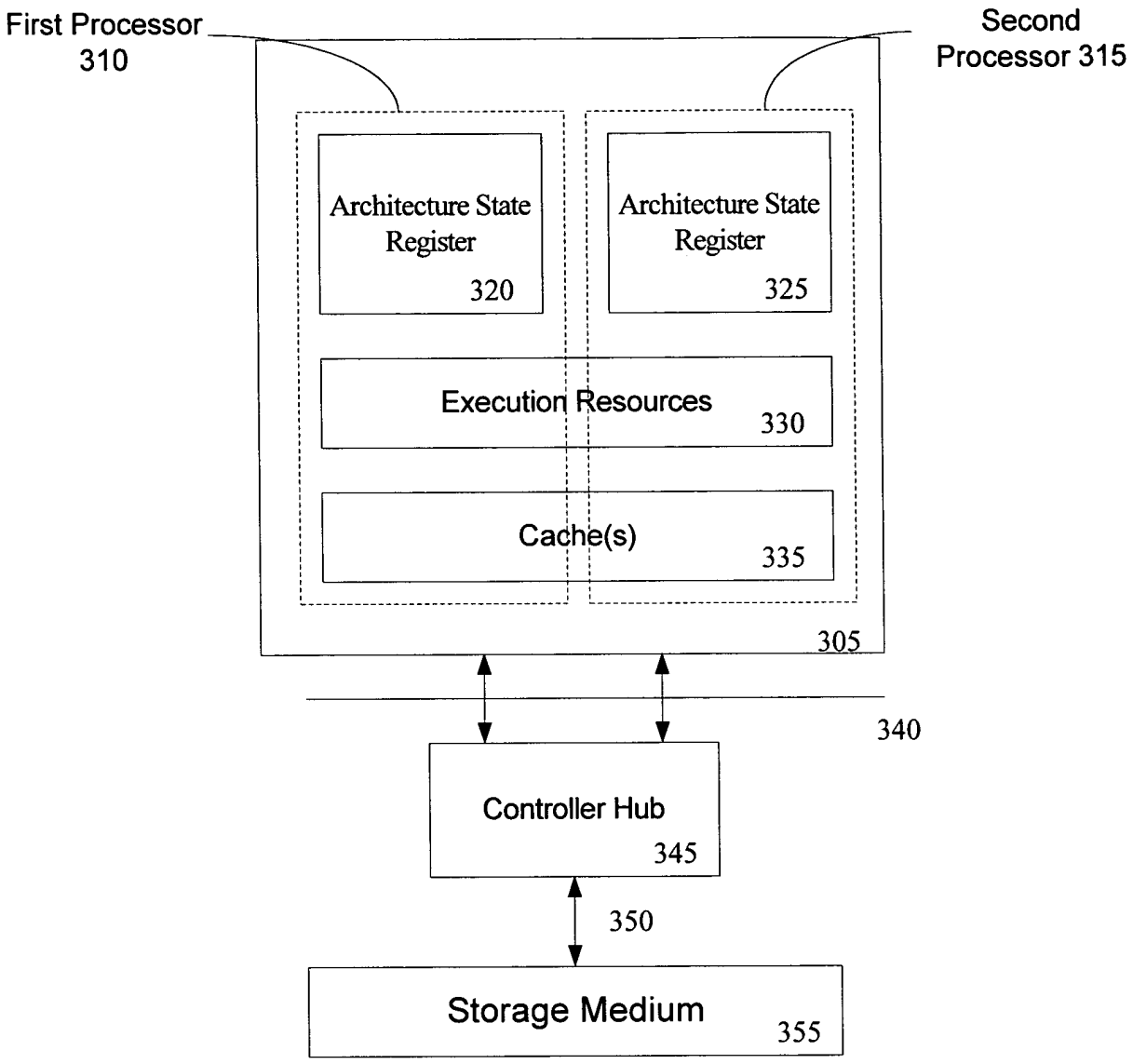
First Processor 310
Second Processor 315
Architecture State Register 320
Architecture State Register 325
Execution Resources 330
Cache(s) 335
305
340
Controller Hub 345
350
Storage Medium 355

FIG. 3

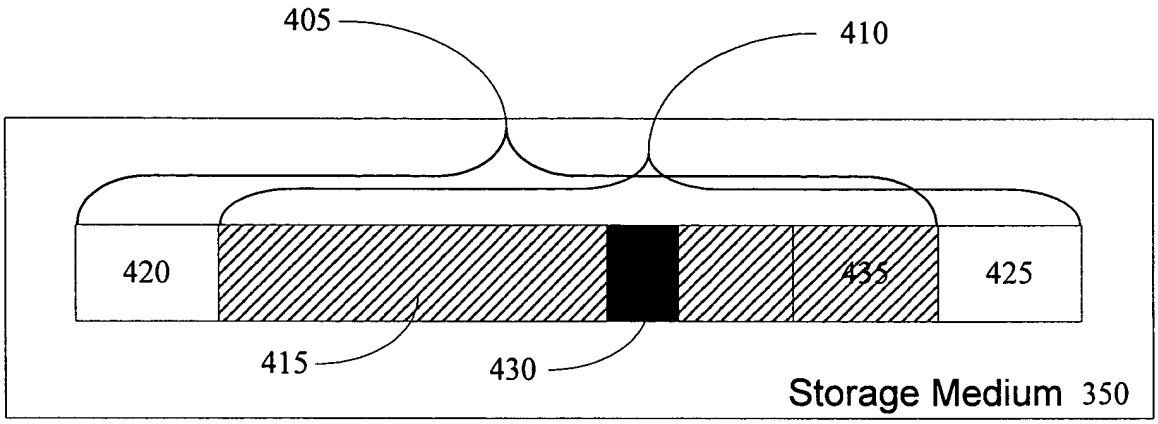

FIG. 4

Value	Meaning
00b 505	The second processor is awake but not in SMI mode, so the first processor needs to wait for the second processor before handling the SMI 520
01b 510	The second processor is sleeping/inactive, so the second processor may proceed to handle the SMI and should handle SMI's on the first processor 525
10b 515	The second processor is awake/active and in SMI, so the first processor may proceed to handle the SMI and should handle SMI's on both the first and second processors 530

430

FIG. 5

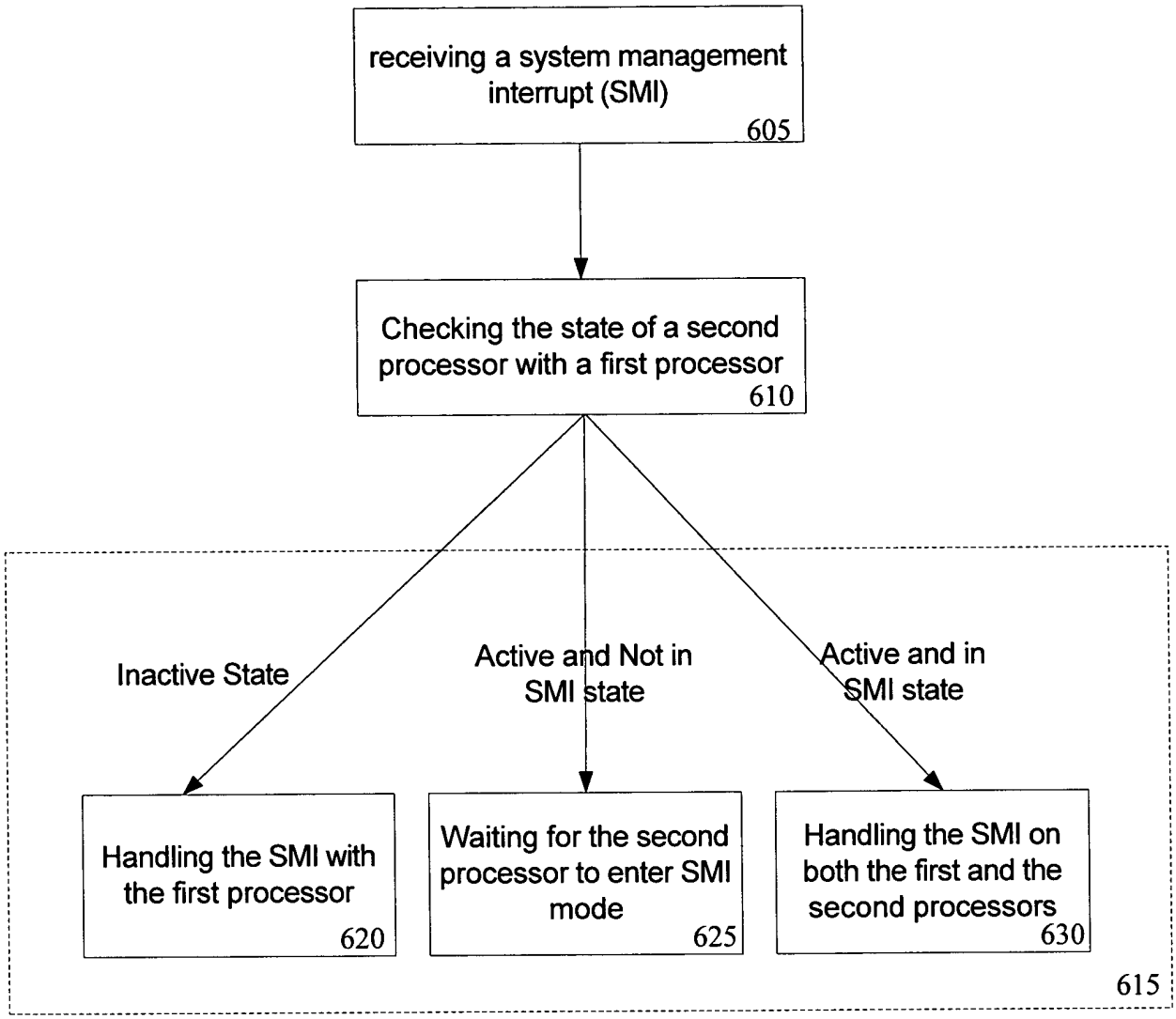
receiving a system management interrupt (SMI)
605
Checking the state of a second processor with a first processor
610
Inactive State
Active and Not in SMI state
Active and in SMI state
Handling the SMI with the first processor
620
Waiting for the second processor to enter SMI mode
625
Handling the SMI on both the first and the second processors
630
615

FIG. 6

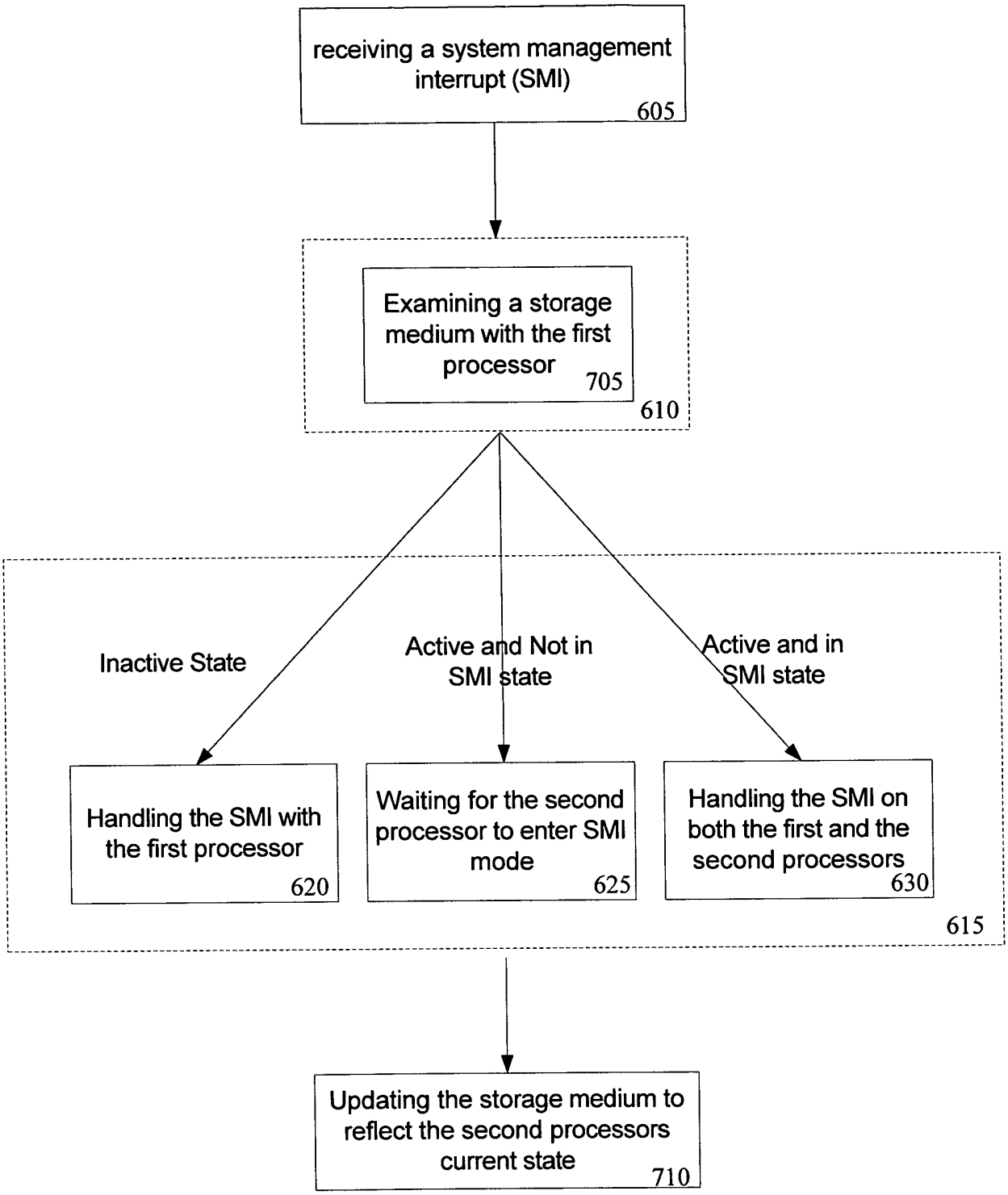
receiving a system management interrupt (SMI)
605
Examining a storage medium with the first processor
705
610
Inactive State
Active and Not in SMI state
Active and in SMI state
Handling the SMI with the first processor
620
Waiting for the second processor to enter SMI mode
625
Handling the SMI on both the first and the second processors
630
615
Updating the storage medium to reflect the second processors current state
710

FIG. 7

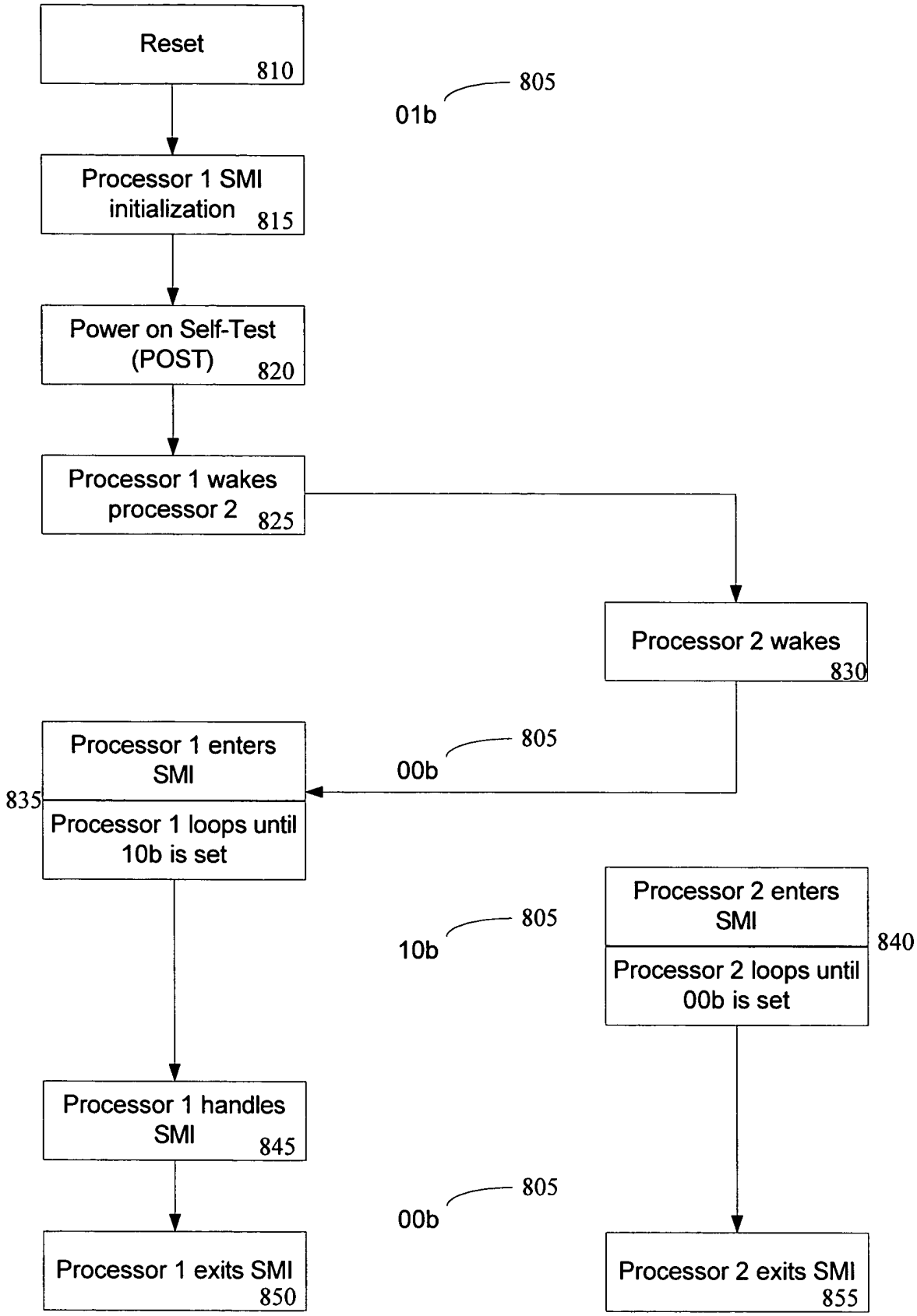
Reset
810
805
01b
Processor 1 SMI initialization
815
Power on Self-Test (POST)
820
Processor 1 wakes processor 2
825
Processor 2 wakes
830
Processor 1 enters SMI
835
Processor 1 loops until 10b is set
805
00b
805
10b
Processor 2 enters SMI
Processor 2 loops until 00b is set
840
Processor 1 handles SMI
845
805
00b
Processor 1 exits SMI
850
Processor 2 exits SMI
855

FIG. 8

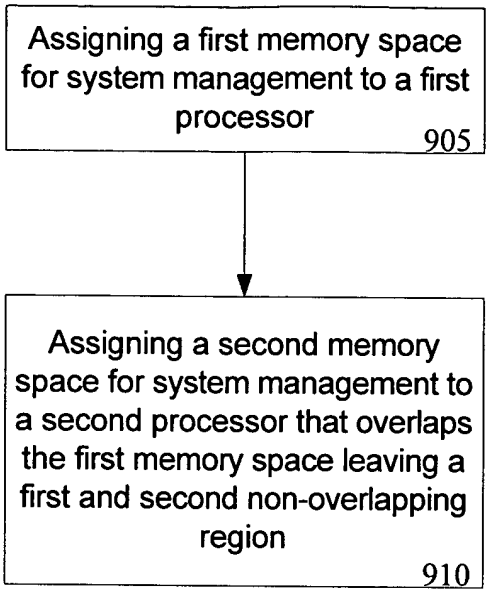
Assigning a first memory space for system management to a first processor
905
Assigning a second memory space for system management to a second processor that overlaps the first memory space leaving a first and second non-overlapping region
910

FIG. 9